APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,415	02/19/2002	James Aweya	57983.000061	2130

7590 05/18/2005	**EXAMINER**
Thomas E. Anderson	SURYAWANSHI, SURESH
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ART UNIT	PAPER NUMBER
2115	

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DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		10/076,415	AWEYA ET AL.
		Examiner	Art Unit	
		Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/29/05 amendments*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

U.S. Patent and Trademark Office

PTOL-326 (Rev. 1-04)   **Office Action Summary**   Part of Paper No./Mail Date 2

DETAILED ACTION

1.   Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-10 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Burns et

al (US Patent No 6,449,291 B1).

4.   As per claim 1, Burns et al disclose

receiving a first timestamp and a second timestamp each indicating a respective time

instance within the network [col. 20, line 66 -- col. 21, line 3; col. 21, lines 7-11; col. 11, lines

23-39; receiving a first timestamp and a second timestamp];

measuring a first time interval between the first timestamp and the second timestamp as

determined by a first clock signal [col. 21, lines 15-16; col. 11, lines 23-39; a headend time

difference (heTimeDiff)];

measuring a second time interval between the first timestamp and the second timestamp

as determined by a second clock signal [col. 21, lines 17-19; col. 11, lines 23-39; a cable modem

difference time (cmTimeDiff)];

generating a difference signal representing a difference between the first time interval and

the second time interval [col. 21, lines 20-22; col. 11, lines 40-44; a clock error]; and

generating the second clock signal based upon the difference signal such that the second

clock signal is synchronized with the first clock signal [col. 21, lines 23-29; col. 11, lines 40-62;

the cable modem generates a synchronized clock signal].

5.   As per claim 20, Burns et al disclose

at least one processor readable carrier [Fig. 5; CPU and computer storage medium RAM

or ROM]; and

instructions carried on the at least one carrier [Fig. 5; RAM];

wherein the instructions are configured to be readable from the at least one carrier by at

least one processor [Fig. 5; RAM or ROM and CPU] and thereby cause the at least one processor

to operate so as to :

receive a first timestamp and a second timestamp each indicating a respective time

instance within the network [col. 20, line 66 -- col. 21, line 3; col. 21, lines 7-11; col. 11, lines

23-39; receiving a first timestamp and a second timestamp];

measure a first time interval between the first timestamp and the second timestamp as

determined by a first clock signal [col. 21, lines 15-16; col. 11, lines 23-39; a headend time

difference (heTimeDiff)];

measure a second time interval between the first timestamp and the second timestamp as

determined by a second clock signal [col. 21, lines 17-19; col. 11, lines 23-39; a cable modem

difference time (cmTimeDiff)];

generate a difference signal representing a difference between the first time interval and

the second time interval [col. 21, lines 20-22; col. 11, lines 40-44; a clock error]; and

generate the second clock signal based upon the difference signal such that the second

clock signal is synchronized with the first clock signal [col. 21, lines 23-29; col. 11, lines 40-62;

the cable modem generates a synchronized clock signal].

6.   As per claim 2, Burns et al disclose delaying the first timestamp by a first delay amount

so as to measure the first time interval between the first timestamp and the second timestamp as

determined by the first clock signal [col. 11, lines 25-34; a headend time difference

(heTimeDiff)].

7.   As per claim 3, Burns et al disclose delaying the first timestamp by a second delay

amount so as to measure the second time interval between the first timestamp and the second

timestamp as determined by the second clock signal [col. 11, lines 35-39; a cable modem time

difference (cmTimeDiff)].

8.   As per claim 4, Burns et al disclose that the first delay amount and the second delay

amount are substantially equal delay amounts [col. 11, lines 23-62; clearly the first delay amount

and the second delay amount will be same when the second clock in synchronism with the first

clock].

9.   As per claim 5, Burns et al disclose initializing the difference signal prior to receiving the

first timestamp and the second timestamp [col. 14, lines 9-16; reset logic].

10.   As per claim 6, Burns et al disclose filtering the difference signal such that the second

clock signal is synchronized with the first clock signal based upon a filtered difference signal

[Fig. 5; col. 8, lines 40-55; col. 12, lines 14-24].

11.   As per claim 7, Burns et al disclose initializing the filtered difference signal prior to

receiving the first timestamp and the second timestamp [col. 14, lines 9-16; reset logic].

12.   As per claim 8, Burns et al disclose controlling the period of a digitally controlled

oscillator based upon the difference signal [col. 8, lines 21-39; all done digitally; col. 12, lines

14-24].

13.   As per claim 9, Burns et al disclose converting the difference signal from a digital

difference signal value into analog difference signal value and controlling the period of a voltage

controlled oscillator based upon the analog difference signal value [col. 3, lines 17-39].

14.   As per claim 10, Burns et al disclose a computer storage medium [Fig. 5; RAM or ROM].

Claim Rejections - 35 USC § 103

15.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

16.   Claims 11-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al

(US Patent No 6,449,291 B1) in view of Rokugo (US Patent No 5,864,248[1]).

17.   As per claim 11, Burns et al disclose

       a receiver for receiving a first timestamp and a second timestamp each indicating a

respective time instance within the network [col. 20, line 66 -- col. 21, line 3; col. 21, lines 7-11;

col. 11, lines 23-39; a modem receives a first timestamp and a second timestamp]; and

a first differencing element for measuring a first time interval between the first timestamp and the second timestamp as determined by a first clock signal [col. 21, lines 15-16; col. 11, lines 23-39; a headend time difference (heTimeDiff)];

a second differencing element for measuring a second interval between the first timestamp and the second timestamp as determined by a second clock signal [col. 21, lines 17-19; col. 11, lines 23-39; a cable modem difference time (cmTimeDiff)];

a third differencing element for generating a difference signal representing a difference between the first time interval and the second time interval [col. 21, lines 20-22; col. 11, lines 40-44; a clock error]; and

a variable oscillator for generating the second clock signal based upon the difference signal such that the second clock signal is synchronized with the first clock signal [col. 21, lines 23-29; col. 11, lines 40-62; the cable modem generates a synchronized clock signal].

Burns et al do not expressly disclose about a phase-locked loop (PLL) associated within the receiver. But a routineer would know that it is well known in the art to utilize a phase-locked loop in a clock synchronization system. However, Rokugo expressly discloses the use of a phase-locked loop circuit in a receiver to reproduce clock signals synchronized with a

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[1] Prior art cited by examiner in the prior office action (dated 12/30/04).

transmitter in a communication system [Fig. 1 and 3; col. 1, lines 9-14; col. 2, line 54 -- col. 3, line 7]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to clock synchronization between transmitter and receiver circuits in a communication network system. Moreover, a routineer would like to use the phase-locked loop disclosed by Rokugo as it is highly stable against amplitude jitters [col. 8, lines 37-41]. Plus, with use of this PLL, a clock can be reproduced accurately and stably [col. 8, lines 52-55] and this PLL circuit can be implemented by a relatively simple circuit configuration [col. 8, lines 61-62].

18.   As per claim 12, Burns et al disclose a first delay element for delaying the first timestamp by a first delay amount so as to measure the first time interval between the first timestamp and the second timestamp as determined by the first clock signal [col. 11, lines 25-34; a headend time difference (heTimeDiff)].

19.   As per claim 13, Burns et al disclose a second delay element for delaying the first timestamp by a second delay amount so as to measure the second time interval between the first timestamp and the second timestamp as determined by the second clock signal [col. 11, lines 35-39; a cable modem time difference (cmTimeDiff)].

20.   As per claim 14, Burns et al disclose that the first delay amount and the second delay amount are substantially equal delay amounts [col. 11, lines 23-62; clearly the first delay amount

and the second delay amount will be same when the second clock in synchronism with the first

clock].

21.   As per claim 15, Burns et al disclose that the second differencing element initializing the

difference signal prior to receiving the first timestamp and the second timestamp [col. 14, lines

9-16; reset logic].

22.   As per claim 16, Burns et al disclose that a loop filter for filtering the difference signal

such that the second clock signal is synchronized with the first clock signal based upon a filtered

difference signal [Fig. 5; col. 8, lines 40-55; col. 12, lines 14-24].

23.   As per claim 17, Burns et al disclose that the loop filter initializes the filtered difference

signal prior to receiving the first timestamp and the second timestamp [col. 14, lines 9-16; reset

logic].

24.   As per claim 18, Burns et al disclose that the variable oscillator is a digitally controlled

oscillator the period of which is controlled based upon the difference signal [col. 8, lines 21-39;

all done digitally; col. 12, lines 14-24].

25.   As per claim 19, Burns et al disclose a digital-to-analog converter [col. 3, lines 17-39].

Response to Arguments

26.   Applicant's arguments with respect to claims 1-20 have been considered but are moot in

view of the new ground(s) of rejection.

Conclusion

27.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

<div style="text-align: right;">
THOMAS LEE
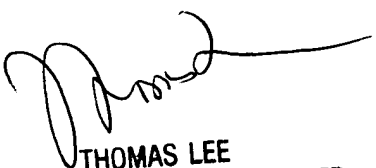SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
May 2, 2005

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100